

CURRENTLY PENDING CLAIMS

- 1 1. (Previously Amended) A system comprising:
2 a memory bus; and
3 a plurality of memory controllers, each memory controller to generate
4 memory requests on the memory bus according to a predetermined priority scheme,
5 at least two of the plurality of memory controllers adapted to generate
6 concurrently pending memory requests on the memory bus.
- 1 2. (Original) The system of claim 1, wherein the predetermined priority
2 scheme comprises a time slot priority scheme.
- 1 3. (Original) The system of claim 1, wherein the predetermined priority
2 scheme comprises a request-select priority scheme.
- 1 4. (Original) The system of claim 1, wherein the memory bus comprises a
2 Rambus channel.
- 1 5. (Original) The system of claim 1, wherein each memory controller
2 generates a memory request during a different predetermined time slot.
- 1 6. (Original) The system of claim 1, wherein the memory bus comprises
2 plural control portions, each of the control portions associated with corresponding time
3 slot priority schemes.
- 1 7. (Original) The system of claim 6, wherein the time slot priority schemes
2 are staggered.
- 1 8. (Original) The system of claim 6, wherein the control portion comprise a
2 row portion and a column portion.

1 9. (Original) The system of claim 1, wherein the memory bus comprises
2 plural portions, each portion associated with a set of memory devices.

1 10. (Original) A system comprising:
2 a memory bus; and
3 a plurality of memory controllers connected to the memory bus, each
4 memory controller to monitor memory requests generated by another memory controller
5 in performing memory-related actions.

1 11. (Original) The system of claim 10, wherein the memory-related actions
2 comprise a read-modify-write transaction.

1 12. (Original) The system of claim 10, wherein the memory-related actions
2 comprise a cache coherency action.

1 13. (Original) The system of claim 10, wherein the memory-related actions
2 comprise a memory request.

1 14. (Original) The system of claim 10, the memory controller to determine if
2 the memory bus is available based on outstanding requests from other memory
3 controllers.

1 15. (Original) A method comprising:
2 providing multiple memory controllers on a memory bus;
3 generating requests, by the memory controllers, on the memory bus; and
4 each memory controller monitoring memory-related actions by at least
5 another memory controller.

1 16. (Original) The method of claim 15, wherein generating the requests
2 comprises generating Rambus command packets.

1 17. (Original) The method of claim 15, wherein generating the requests
2 comprises the memory controllers generating the requests one at a time according to a
3 predetermined priority scheme.

1 18. (Original) The method of claim 17, wherein generating the requests
2 comprises generating the requests according to a time slot priority scheme.

1 19. (Original) The method of claim 17, wherein generating the requests
2 comprises generating the requests according to a request-select priority scheme.

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1 20. (Previously Amended) The method of claim 15, further comprising each
2 memory controller determining when to generate a memory request based on the
3 monitoring.

1 21. (Previously Amended) The method of claim 15, further comprising each
2 memory controller determining if a lock has been asserted due to presence of a read-
3 modify-write transaction.

1 22. (Previously Amended) The method of claim 15, further comprising each
2 memory controller performing a cache coherency action based on the monitoring.

1 23. (Original) An article comprising one or more storage media containing
2 instructions that when executed cause a memory controller to:
3 monitor memory requests from another memory controller on a memory
4 bus;
5 determining if a memory request can be generated on the memory bus
6 based on the monitoring.

1 24. (Previously Added) The system of claim 1, wherein the plurality of
2 memory controllers are connected to the memory bus.

1 25. (Previously Added) The system of claim 1, wherein one of the at least two
2 memory controllers is adapted to generate its memory request on the memory bus before
3 data is returned for the memory request of the other one of the at least two memory
4 controllers.

1 26. (Previously Added) The system of claim 10, wherein at least two of the
2 memory controllers are adapted to generate concurrently pending memory requests on the
3 memory bus.

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1 27. (Previously Added) The system of claim 26, wherein one of the at least
2 two memory controllers is adapted to generate its memory request on the memory bus
3 before data is returned for the memory request of the other one of the at least two
4 memory controllers.

1 28. (Previously Added) The method of claim 15, wherein generating the
2 requests on the memory bus comprises at least two of the memory controllers generating
3 concurrently pending requests on the memory bus.

1 29. (Previously Added) The method of claim 28, wherein generating
2 concurrently pending requests comprises one of the at least two memory controllers
3 generating its request before data is returned for the request of the other of the at least
4 two memory controllers.

1 30. (Previously Added) The article of claim 23, wherein the memory
2 controllers are connected to the memory bus.
